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A 2.3/3.3-GHz Dual Band Low Noise Amplifier Using Switchable Load Inductor in 0.18-μm CMOS Technology

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Abstract

In this paper, the dual band low noise amplifier is designed in 0.18-μm CMOS technology. By combining the proposed switchable load inductor for gain controlling and the conventional inductive source degeneration topology, narrow band gain and good impedance matching are achieved at 2.3/3.3-GHz frequency bands. The new mathematical analysis of low noise amplifier design is derived to define the component parameters of the proposed circuits. The proposed low noise amplifier exhibits gain of 17.18 dB and 15.5 dB, and noise figure of 2.67 dB and 2.52 dB at the two frequency bands, respectively.

Abstrak

Penguat Derau Rendah Pita Ganda 2,3/3,3-GHz dengan Menggunakan Induktor Beban yang dapat Dialihkan di dalam Teknologi CMOS 0,18-μm. Pada paper ini, *dual band low noise amplifier* didesain menggunakan teknologi CMOS 0.18-μm. Dengan mengkombinasikan usulan *switchable load inductor* sebagai pengendali *gain* dan topologi konvensional *inductive source degeneration*, gain dengan lebar yang sempit dan kesesuaian impedansi yang baik dapat dicapai pada frekuensi 2.3/3.3-GHz. Analisa matematika rangkaian yang baru pada desain rangkaian *low noise amplifier* telah dijabarkan untuk menentukan parameter-paramter komponen rangkaian yang diusulkan. *Low noise amplifier* yang didesain menghasilkan gain sebesar 17.18 dB dan 15.5 dB, serta noise figure sebesar 2.67 dB dan 2.52 dB pada dua pita frekuensi, secara berurutan.

Keywords: dual band LNA, switchable load inductor, inductive source degeneration, 0.18-μm CMOS Technology

1. Introduction

Nowadays, the Internet of Things (IoT) changes the paradigm about the technology interaction in daily life. Many applications such as smart city concept, home automation, and health monitoring based on IoT have been viral in recent years [1]. The utilization of IoT platforms are able to reduce operation cost and dependence on human intervention. However, the technology interaction based on IoT is not suitable if applied in wired communication. Many studies have attempted to develop these systems by using short range and long range wireless communications. Therefore, the rapid development in the field of IoT is not regardless of the rapid progress in the broadband wireless communication as its key technology.

The broadband wireless communication system is expected to provide flexible delivery data over multiple platform technologies [2]. Hence, wideband or multi band transceivers become more familiar in the wireless communication fields [3]. The multiband approach decreases the power consumption than the single band scheme, significantly. However, it needs a reliable block circuits. One of the most important block circuits in the wireless transceiver system is low noise amplifier (LNA). As a part of the front-end receiver, a powerful LNA circuits can produce good input matching, low noise figure and sufficient small-signal gain with high linearity [4]. This is a big challenge for microwave researchers, because those performances are trade-offs, especially for LNA operated in multi band frequency.

In this work, a single narrow band low noise amplifier (LNA) topology is adopted to design dual band LNA. The wide-band LNA is promising, however the topology is vulnerable to interferences from undesired applications due to its limited linearity [5] and noise performance [6]. Though the LNA topology using two narrow bands in parallel [7] has good performance at either frequency

band, it dissipates high power and requires a large chip size [8]. The other approaches adopting two difference input circuits [9] or a concurrent dual-band matching circuit [10] are compact and consume smaller power than the conventional design. However, they still occupy a large chip area due to the necessity of more inductors in the circuits.

To control the peak gain of dual band LNA (DB-LNA), a new switchable load inductor (SLI) is proposed. The conventional inductive source degeneration is adopted as a basic structure to realize good impedance matching in narrow band applications. The new mathematical analysis for LNA design procedures is derived to determine the optimum circuit parameters.

This paper is organized as follows. In Section II, we will brief discuss the detailed design of the proposed LNA. The simulation results and performance comparison with recently published works are shown in Section III. Conclusions are given in Section IV.

2. Methods

LNA Topology and Circuit Design.
The proposed DB-LNA schematic is illustrated in Fig. 1, where two parallel transistors are designed for dual band frequencies, 2.3-GHz and 3.3-GHz. Turning on the switch (S_w) increases the size of the common-source transistor (M_1 and M_2). This operation will move the resonance frequency from the higher band (3.3 GHz) to the lower band (2.3 GHz). The optimized size of the M_1 and M_2 can be determined as follows [11]:

$$W_{opt} = \frac{3}{2\omega_0 L C_{ox} R_s Q_{L,OPT}} \quad (1)$$

in which, $Q_{L,opt}$ of the input LNA is around 4.5 (i.e., average of 3.5 and 5.5) [12]. In our design, the optimum current-source transistor size for 3.3 GHz and 2.3 GHz are 204 μm and 290 μm, respectively. Since the low-frequency band mode (2.3 GHz) is obtained by parallel connecting of two common-source transistors (M_1 and M_2), the W_{opt} of M_2 can be calculated by subtracting 204 μm from 290 μm.

According to the Fig. 1, the input impedance Z_{in} of the proposed DB-LNA is given by

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs1}} + \left(\frac{g_{m1}}{C_{gs1}}\right) L_s \quad (2)$$

Where gm_1 and Cgs_1 is the transconductance and the gate-source capacitance of transistor M_1. The source-degenerative inductance of L_S can be determined by the following equation:

$$R_s = \left(\frac{g_{m1}}{C_{gs1}}\right) L_s = 50\ \Omega \quad (3)$$

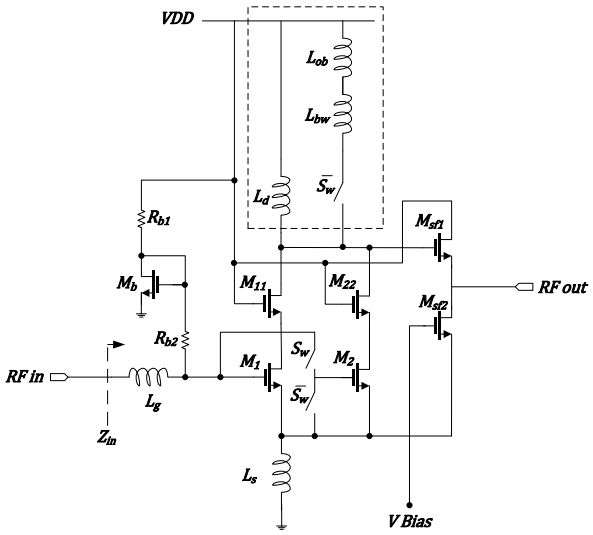


Figure 1. Complete Schematic of the Proposed LNA

Based on (2), the input return loss S_{11} of the DB-LNA can be expressed as,

$$S_{11} = \frac{Z_{in} - R_s}{Z_{in} + R_s}$$

$$= \frac{s(L_g + L_S) + \frac{1}{sC_{gs1}}}{s(L_g + L_S) + 2.\frac{g_{m1}L_s}{C_{gs1}} + \frac{1}{sC_{gs1}}}$$

$$= \frac{s^2 + \frac{1}{C_{gs1}(L_g + L_S)}}{s^2 + 2.\frac{g_{m1}L_s}{C_{gs1}(L_g + L_S)}.s + \frac{1}{C_{gs1}(L_g + L_S)}}$$

$$= \frac{s^2 + {\omega_o}^2}{s^2 + \xi s + {\omega_o}^2} \quad (4)$$

The small signal model of the input stage of the proposed DB-LNA is depicted in Fig. 2(a). The switch (S_w) in Fig. 1 is represented by the transmission gate. When the transmission gate is switched on, the resonant frequency will be shifted to a lower band due to the increase of gate-to-source capacitance. In this work, we assume that the on-resistance of the transmission gate can be neglected. As described previously, the input resistance of the inductive source degeneration topology is $(g_m/C_{gs})L_s = (g_{m1}/C_{gs1})L_s$ for the switch-off case as shown in Fig. 2(b). For the switch-on case as shown in Fig. 2(c), the input resistance becomes $[(g_{m1} + g_{m2})/(C_{gs1} + C_{gs2})]L_s$ = 50 ohm. Where

$g_m = (g_{m1} + g_{m2})$ is the equivalent transconductance and $C_{gs} = (C_{gs1} + C_{gs2})$ is the equivalent gate-to-source capacitance of the two parallel-connected transistors. The condition $\omega R_{on} C_{gs2} \ll 1$ is required such that the transmission gate's on-resistance has insignificant effect on the analysis. Hence, the following analysis holds for both 2.3 and 3.3 GHz bands.

The switchable load inductor (SLI) configuration is proposed to control the peak gain of the proposed LNA as depicted in dashed-line rectangle on Fig. 1. For the low-frequency band mode, the $\overline{S_w}$ is switched-off, hence the peak gain will be only determined by on-chip inductor (L_d). Otherwise, the peak gain for the high-frequency band mode is determined by the bondwire inductor (L_{bw}) in series connection with the on-board inductor (L_{ob}), as well as in parallel connection with L_d. In this proposed configuration, the on-resistance of $\overline{S_w}$ contributes a parasitic resistance that will degrade the Q-factor of L_{bw} in series connection with L_{ob}. Hence, in the switch-on case, the Q-factor of the series connection inductor is similar to the Q-factor of L_d. Therefore, the signals will pass through the parallel inductor connection.

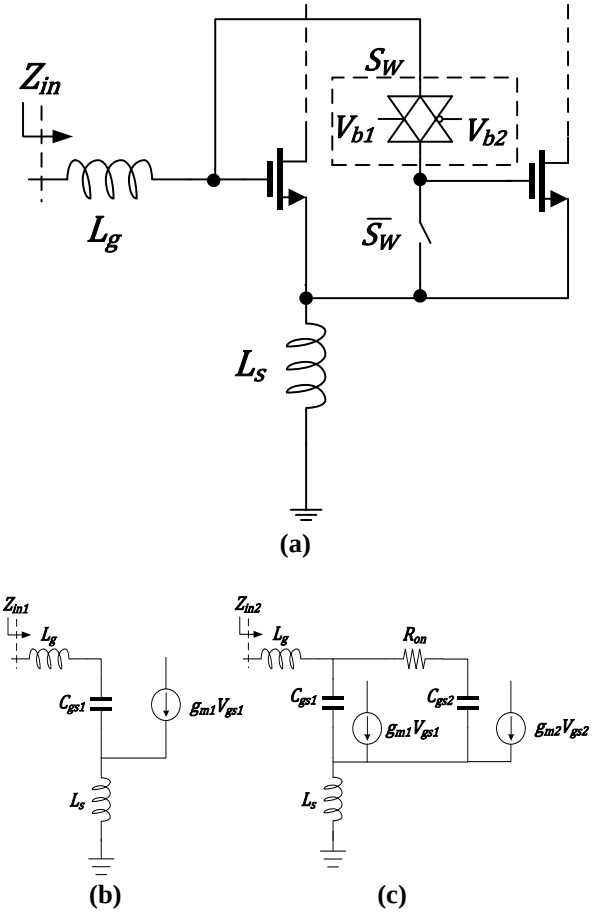


Figure 2. (a) Small Signal Model of the Input Stage of The Proposed LNA, (b) Switch-off Circuit Model, (c) Switch-on Circuit Model

According to the reason, the on-chip inductor in parallel connection with the on-board inductor prefers to be implemented instead of another parallel combination (i.e. on-chip inductor in parallel with on-chip inductor or on-board inductor in parallel with on-board inductor) to obtain similar gain performance between both modes of DB-LNA. To demonstrate the parasitic effects of the L_{bw} and the L_{ob}, the equivalent circuit is shown in the Figs. 3(a) and 3(b), respectively.

For analyzing the gain performance of the proposed LNA, we start to analysis the common gate (M_{11}) transistor first. The small signal model of the M_{11} is shown in Fig. 4(a).

By KCL and KVL,

$$\begin{bmatrix} g_{ds2} & \dfrac{g_{m2} + g_{ds2}}{C_{gs2}s} + 1 \\ -1 & \dfrac{L_d s + r_{Ld}}{1 + (L_d s + r_{Ld}) C_L s} \end{bmatrix} \begin{bmatrix} V_0 \\ i_1 \end{bmatrix}$$

$$= \begin{bmatrix} 1 \\ \dfrac{L_d s + r_{Ld}}{1 + (L_d s + r_{Ld}) C_L s} \end{bmatrix} i \qquad (5)$$

where r_{Ld} is parasitic resistance of L_d. Then, the transfer function of V_0 respect to i, can be expressed easily.

By KCL in Fig 4(b), i_2 can be expressed as,

$$i_2 = g_{ds1}\left(-V_{gs2} - \left(i + V_{gs1} C_{gs1} s\right)(L_S s + r_{Ls})\right) \qquad (6)$$

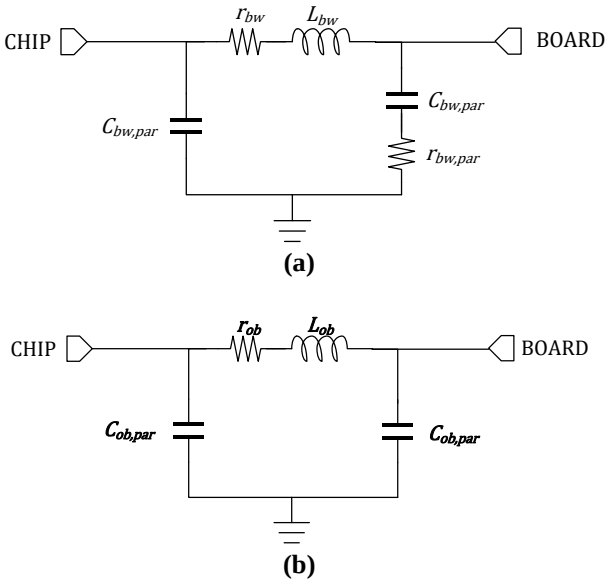


Figure 3. (a) Equivalent Circuit for The Bondwire (L_{bw}), (b) The On-board Inductor (L_{ob})

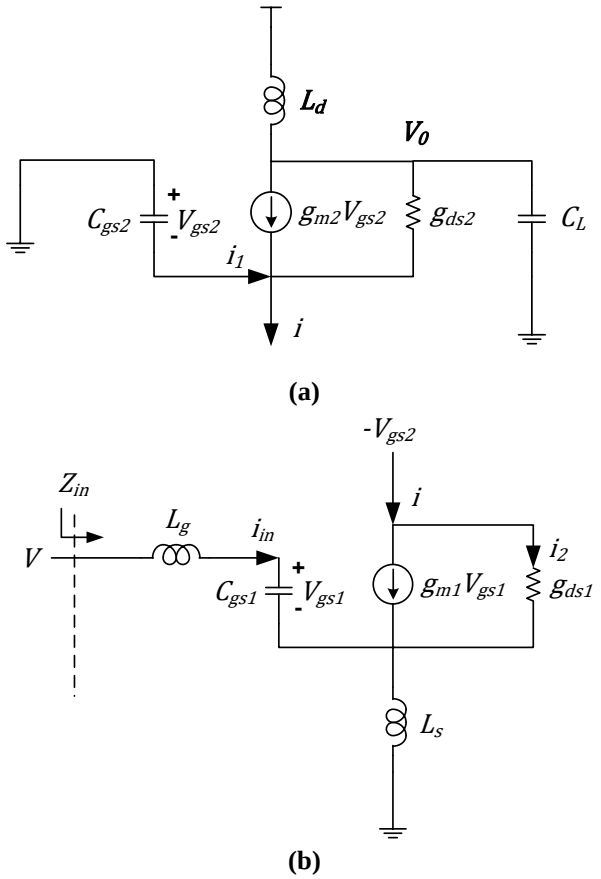


Figure 4. (a) Common Gate Transistor (M_{11}) Equivalent Circuit Model, (b) Small Signal of Transistor M_1

Where r_{LS} is parasitic resistance of L_S. From Fig. 4(a), we find that $V_{gs2} = i_1/(C_{gs2}s)$. Therefore,

$$V_{gs2} = \frac{iD(s)}{A(s)} \tag{7}$$

Let,

$$A(s) = (L_d s + r_{Ld}) g_{ds2} C_{gs2} s + (1 + (L_d s + r_{Ld}) C_L s) * \left(g_{m2} + g_{ds2} + C_{gs2} s\right) \tag{8}$$

$$D(s) = 1 + (L_d s + r_{Ld}) C_L s + (L_d s + r_{Ld}) g_{ds2} \tag{9}$$

Therefore, i_2 can be written as,

$$i_2 = -g_{ds1}\left(i\left(\frac{D(s)}{A(s)} + (L_S s + r_{Ls})\right)\right) - g_{ds1}(i_{in}(L_S s + r_{Ls})) \tag{10}$$

From Fig. 4(b), we notice that

$$i_2 = i - i_{in}\frac{g_{m1}}{C_{gs1}s} \tag{11}$$

Therefore,

$$i = \frac{i_{in}\left(g_{m1} - g_{ds1}C_{gs1}(L_S s + r_{Ls})s\right)}{\left[1 + g_{ds}\left(\frac{D}{A} + (L_S s + r_{Ls})\right)\right] C_{gs1} s} \tag{12}$$

The value of i_{in} can be derived by KVL in Fig. 4(b),

$$V = i_{in}\left((L_g s + r_{Lg}) + \frac{1}{C_{gs1}s}\right) + (L_S s + r_{Ls})(i_{in} + i) \tag{13}$$

where r_{Lg} is parasitic resistance of L_g. Finally, the input impedance of the circuit Z_{in} can be found as follows

$$Z_{in} = \frac{V}{i_{in}}$$

$$Z_{in} = \left\{(L_g s + r_{Lg}) + (L_S s + r_{Ls})\right\} + \frac{1}{C_{gs1}s} + \frac{(L_S s + r_{Ls})\left(g_{m1} - g_{ds1}(L_S s + r_{Ls})C_{gs1}s\right)}{sC_{gs1}\left(1 + g_{ds1}\left(\frac{D}{A} + (L_S s + r_{Ls})\right)\right)} \tag{14}$$

Next, we ignore r_{Ld}, r_{Lg} and r_{Ls} because their values are very small. Let ω_0 be the frequency of the peak gain where $1 - L_d C_L {\omega_0}^2 = 0$ and for input matching $1 - \left\{(L_g) + (L_S)\right\} C_{gs1} {\omega_0}^2 = 0$, thus

$$\frac{D(j\omega_0)}{A(j\omega_0)} = \frac{1}{j\omega_0 C_{gs2}} \tag{15}$$

Then,

$$Z_{in}(j\omega_0) = \frac{(j\omega_0 L_S)\left\{g_{m1} - g_{ds1}(j\omega_0 L_S)C_{gs1}.j\omega_0\right\}}{j\omega_0 C_{gs1}\left[1 + g_{ds1}\left(\frac{1}{j\omega_0 C_{gs2}} + j\omega_0 L_S\right)\right]} \tag{16}$$

Next, in order to obtain the real input impedance, *50Ω*, ${C_{gs1}\omega_0}^2$ is replaced by $1/(L_s + L_g)$. Therefore, Z_{in} at the operating frequency can be determined as follows,

$$Z_{in}(j\omega_0) = \frac{L_S\left(g_{m1} + g_{ds1}\left(\frac{L_s}{L_s + L_g}\right)\right)}{C_{gs1}\left[1 - jg_{ds1}\left(\frac{1 - \frac{L_s C_{gs2}}{(L_g + L_s)C_{gs1}}}{\omega_0 C_{gs2}}\right)\right]} \tag{17}$$

At the operating frequency by assuming that $g_m \gg g_{ds1}$, $g_{ds1} \ll 1$ and $C_{gs2} \ll C_{gs1}$, the real input impedance (Z_{in}) in (18) is similar with the simple expression in (3).

From Fig. 4(b), let $Z_{in}(j\omega_0)$ be Z_0 from (17), i_{in} can be expressed as,

$$i_{in} = \frac{V_{in}}{Z_0 + (L_g + L_S)s + \frac{1}{C_{gs1}s} + \frac{L_s(g_{m1} - g_{ds1}L_sC_{gs1}s^2)}{C_{gs1}\left(1 + g_{ds1}\left\{\frac{D}{A} + L_ss\right\}\right)}} \quad (18)$$

Hence, by combining (12) and (18)

$$i = \frac{1}{\left(\left[1 + g_{ds1}\left(\frac{D}{A} + L_Ss\right)\right]C_{gs1}s\right)} * \frac{V_{in}(g_{m1} - g_{ds1}L_SC_{gs1}s^2)}{(Z_0C_{gs1}s + \frac{s^2}{{\omega_0}^2} + 1 + \frac{L_ss(g_{m1} - g_{ds1}L_sC_{gs1}s^2)}{\left(1 + g_{ds1}\left(\frac{D}{A} + L_ss\right)\right)})} \quad (19)$$

The overall transconductance becomes,

$$\frac{i}{V_{in}} = \frac{1}{\left[1 + g_{ds1}\left(\frac{D}{A}L_Ss\right)\right]} * \frac{g_{m1} - g_{ds1}C_{gs1}L_Ss^2}{\left[\frac{s^2}{{\omega_0}^2} + Z_0C_{gs1}s + 1\right] + L_Ss[g_{m1} - g_{ds1}C_{gs1}L_Ss^2]} \quad (20)$$

Finally, from the transfer function equation of V_0 respect to i derived from (5) and (20), the voltage gain (A_v) of the proposed LNA can be simplified as,

$$\frac{V_0}{V_{in}} = \frac{-j(g_{m2} + g_{ds2})\left(g_{m1} + g_{ds1}\frac{L_s}{(L_s + L_g)}\right)}{(g_{ds1}C_{gs2}L_S{\omega_0}^2 - 2jC_{gs2}\omega_0 - g_{ds1})\frac{g_{ds2}Z_o}{(L_g + L_s)}} \quad (21)$$

Furthermore, the mathematical noise analysis of the proposed LNA is derived. As depicted in Fig. 5, the equivalent noise model from inductive source degeneration LNA topology can be written as

$$Z_{in} = r_{Lg} + r_g + r_{nqs} + r_{ss} + r_{Ls} + \frac{g_{m1}L_S}{C_{gs}} \quad (22)$$

where r_{Lg}, r_g, r_{nqs}, r_{ss}, r_{Ls} are gate inductor (L_g) resistance, gate resistance, non-quasi static effect of the transistor, source resistance, and source inductor (L_S) resistance respectively.

Some previous works [13]-[15] have modelled the noise sources for RF CMOS transistors as:

$$\overline{i^2_{nd}} = 4kT\gamma g_{d0} \quad (23)$$

$$\overline{i^2_{ng}} = \frac{4kT\delta\omega^2{C_{gs}}^2}{5g_{d0}} \quad (24)$$

In which, $g_{d0} = (g_m/\alpha)$ represents the MOSFET output conductance at zero drain-source bias, for short channel $\alpha \leq 1$ [15]. γ, δ are the coefficients of transistor's channel noise and gate noise, respectively. Furthermore, since the proposed LNA works at low frequencies, the noisy gate current is ignored in this work [13], [16].

Recall that the noise factor (*F*) for an amplifier is defined as the total output noise power divided by the total output noise due to the input source resistance.

First, the transconductance of the circuit of the input stage is evaluated to make sure that the output noise of the LNA is driven by a *50-Ω* source.

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{C_{gs1}(L_g + L_S)s^2 + (C_{gs}R_S + L_Sg_{m1})s + 1} = \frac{\omega_T}{j\omega_0(R_S + \omega_TL_S)} = \frac{\omega_T}{2j\omega_0R_S} \quad (25)$$

where Q_{in} is effective *Q* of the amplifier's input circuit.

From (23), we can derive that the output noise power spectral density arising from this source is

$$S_{o,i_{nd}}(\omega_0) = 4kT\gamma g_{d0} \quad (26)$$

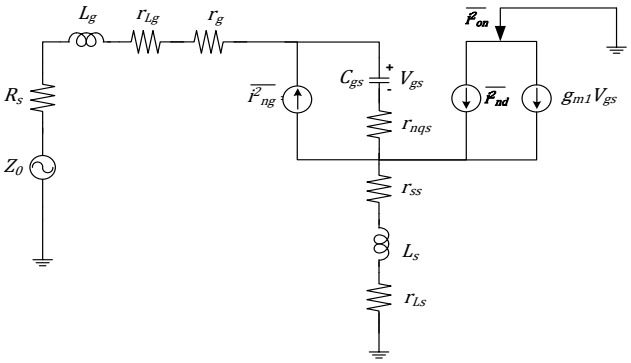


Figure 5. Noise Model of Inductive Source Degeneration Configuration

In addition, the output noise power spectral density due to the input source resistance ($S_{o,SR}(\omega_0)$) can be written by,

$$S_{o,SR}(\omega_0) = S_{SR}(\omega_0){G_{m,eff}}^2$$

$$= \frac{4kT{\omega_T}^2}{{\omega_0}^2 R_S\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \quad (27)$$

Then, the output noise power spectral density due to parasitic resistance ($S_{o,r_{par}}(\omega_0)$)can be represented by

$$S_{o,r_{par}}(\omega_0) = \frac{4kT\left(r_{Lg}+r_g+r_{SS}+r_{Ls}\right){\omega_T}^2}{{\omega_0}^2{R_S}^2\left(1+\frac{\omega_T L_s}{R_S}\right)^2} \quad (28)$$

Hence, the total output noise power density is the sum of (26), (27) and (28). Therefore, the noise figure of the proposed LNA can be approximated by:

$$F = 1 + \frac{r_{Lg}+r_g+r_{SS}+r_{Ls}}{R_S} + 4\gamma g_{d0} R_S\left(\frac{\omega_0}{\omega_T}\right)^2 \quad (29)$$

3. Results and Discussion

The proposed DB-LNA is designed in 0.18-µm CMOS technology and simulated by considering all the parasitic components for an on-board measurement. Fig. 6 shows the comparison between the calculation and the post-layout simulation results to verify the mathematical analysis for the input impedance (S_{11}) in (4), the voltage gain (A_v) in (21) and the noise figure (NF) in (29), respectively. The circuit parameters are: g_{m1} = 63.1 *mS*, g_{m2} = 63.1 *mS*, C_{gs1} = 170.02 *fF*, C_{gs2} = 93.6 *fF*, g_{ds1} = 0.002 *mS*, g_{ds1} = 0.001 *mS*, L_S = 1.3 *nH*, L_g = 1.3 *nH*, L_d = 7.4 *nH*.

As shown in Figs. 6(a) and 6(b), the small difference between the calculation and simulation is the bandwidth. In the simulation, the uncountable parasitics of the inductor decreases the Q [17]. Since the fractional -3 dB bandwidth of S_{11} and S_{21} in inductive source degeneration topology is inversely proportional to its Q-factor [12], [18], the bandwidth of the proposed LNA in the simulation is wider than in the calculation. For the noise figure analysis verification, we use: $\gamma = 1.15$, $\alpha = 0.75$, and $\delta = 1.33$. The contribution of γ and δ for 0.18-µmCMOS technology have been plotted in previous work [19] and [14], respectively.

Fig. 7 shows the simulated S_{11}, S_{21}, and NF for both frequencies. The input return loss (S_{11}) is below -10 dB, the small signal gain (S_{21}) of 15.5~17.8 dB is obtained as depicted in Figs. 7(a) and 7(b), respectively. A low noise figure (NF) is achieved for low-frequency band mode of 2.67~2.71 dB and for high-frequency band mode of 2.52~2.54 dB, as illustrated in Fig. 7(c). The input third intercept points (IIP_3), S_{11}, S_{21}, NF and power consumption are summarized and compared with the previous published works in Table 1.

A figure of merit (FOM) depicted in Table I is used to compare between the proposed LNA and recently published LNAs. This FOM is proposed in [20], i.e.,

$$FOM = \frac{Gain[abs]}{(NF-1)[abs].P_{DC}[mW]} \quad (30)$$

The chip area is 0.9 mm^2 including the pads with a micrograph shown in the Fig. 8.

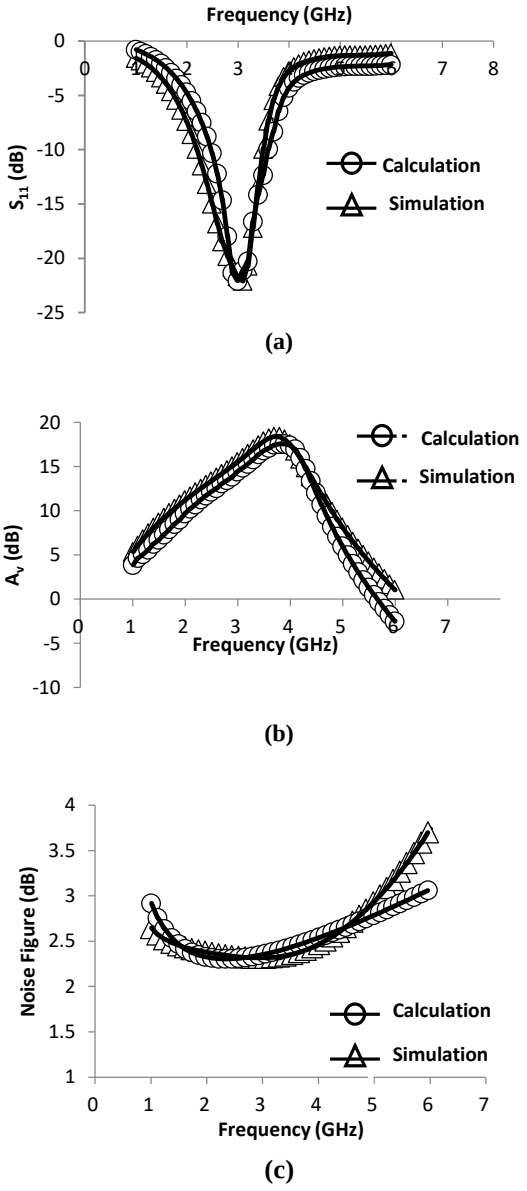
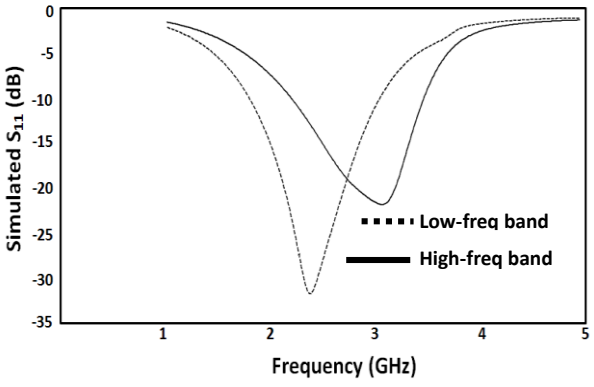


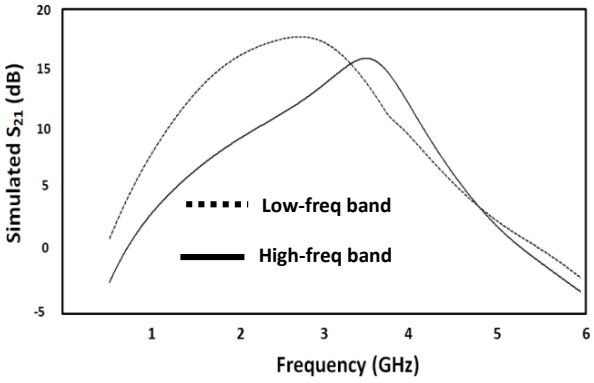
Figure 6. Calculation and Simulation Comparison:(a) Input Matching (S11), (b) Voltage Gain (Av), (c) Noise Figure (NF)

Table 1. Performance Comparison

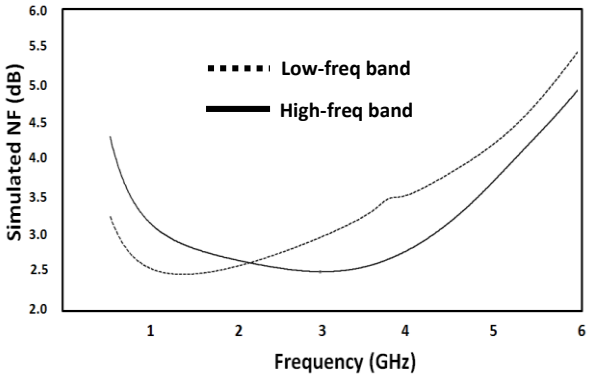
Ref.	This Work		[21]	[22]	[23]	[24]
	Low-freq band	**High-freq band**				
Freq (*GHz*)	**2.3**	**3.3**	2.4	0.9	0.9	0.96
S_{11} (*dB*)	**-32**	**-16.8**	-20	-11	-14	-10
S_{21} (*dB*)	**17.8**	**15.8**	13	17.5	17	13
NF (*dB*)	**2.6**	**2.5**	3.6	2.05	3.4	3.6
IIP_3 (*dBm*)	**-13.4**	**-12.3**	-3	-6	-5.1	-10
P1dB (*dBm*)	**-24.2**	**-23.3**	-	-	-	-18
P_{DC} (*mW*)	**16.3**	**11.8**	7.2	21.6	12.8	0.72
Area (mm^2)	**0.9**	**0.9**	0.56	-	0.35	2.6
FOM	**0.64**	**0.89**	0.69	0.77	0.54	0.60



(a)



(b)



(c)

Figure 7. Simulated: (a) Input Matching (S11), (b) Gain (S21) and (c) Noise Figure (NF)

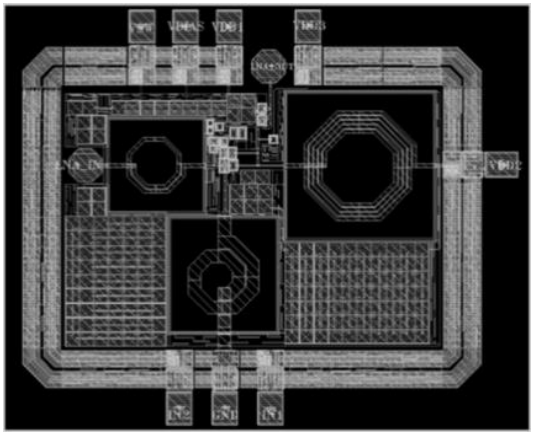


Figure 8. Chip Layout

4. Conclusion

A 2.3/3.3-GHz dual band LNA is proposed by combining switchable load inductor for gain controlling and inductive source degeneration topology. The mathematical analysis verification for input impedance (S_{11}), voltage gain (A_v) and noise figure (*NF*) show that the derived equation agrees well with that obtained from the simulation. For both of bands, the proposed DB-LNA can compete with the other published and implemented DB-LNA based on on-board measurement in terms of S_{21}, *NF*, IIP_3, and the power consumption.

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